IN THE CLAIMS

Claims 47-55 are amended and new claims 56-64 are added.

All claims as currently pending are presented by way of the attached document entitled AMENDED CLAIMS in Serial No. 07/933,891.

Also attached hereto is a check for $74.00 (Check #4590) to cover the fee for the added claims.

IN RE TITLE

Examiner holds that "The title of the invention is not descriptive". Applicant proposes the following new title.

COMPACT FLUORESCENT LAMP ASSEMBLY

REMARKS

Examiner rejected claims 51-52 and 54-55 under 35 USC 102b as being anticipated by Dale et al. ("Dale").

Applicant traverses Examiner's rejections on basis of the following analysis of exemplary claim 52, which analysis applies to claim 51 as well. (In re claim 51, note the following recitation: "the first transistor being operative to prevent the flow of current ... during the second and fourth time segments", i.e., the up-slopes & down-slopes of Canup's Fig. 4.)

(a) Exemplary claim 52 includes:

"... ballast means ... including a periodically conducting transistor having ... a pair of output terminals across which exists a periodically varying transistor voltage ... characterized by having four time segments: (i) a first time segment during which the magnitude of the transistor voltage remains at a first ... constant level, (ii) a second time segment during which the magnitude of the transistor voltage increases in a ... gradual manner ... the transistor conducting current in its forward direction during at least part of the first time segment but not during most of the second time segment". (Emphasis added)

This feature is neither described nor suggested by Dale.

If Examiner were to remain of a contrary opinion, he is requested to point out exactly where and/or how Dale suggests this feature.

In this connection, Applicant informs Examiner to the effect that the above-identified feature is not a result of "inherent functions of the Dale et al. device", nor of inverters in general. For instance, in Canup's Square Wave Oscillator, it is clear that current flows through each switched transistor all during the period when the collector-to-emitter voltage is increasing; which is to say: while the transistor is in the process of being switched off. In actual fact, until the voltage across the switched transistor reaches its maximum level, the transistor current has no place to flow except through the transistor. Even when "increasing switching time of said transistors" (see Canup's column 2, lines 3-7), current must flow through the switched transistor during the whole period while being switched off (i.e., the period between lines 45 and 46 in Fig. 4, or until maximum transistor voltage is attained).

Examiner rejected claims 47-49 and 53 under 35 USC 103 as being unpatentable over Dale in view of Canup.

Applicant traverses these rejections for the following reasons.

(b) Exemplary claim 47 includes:

"... inverter means including: (i) a first transistor characterized by conducting current during the first time segment but not at other times ... the duration of the first time segment being ... shorter than half the duration of the fundamental period".

This feature is neither described nor suggested by either Dale or Canup.

If Examiner were to remain of a contrary opinion, he is requested to point out exactly where and/or how Dale and/or Canup suggests this feature.

In this connection, Examiner's attention is directed to Applicant's Fig. 3A, which shows that the duration of the first time segment is distinctly shorter than half the duration of the total fundamental period. On the other hand, with reference to discussion presented in the first paragraph on this page, it is clear that each of Canup's transistors conducts current during the equivalent of Applicant's first segment as well as during the equivalent of Applicant's second segment. That is, with reference to Canup's Fig. 4, a complete half period consists of one horizontal segment and one sloping segment; and, as a matter of plain fact, each one of Canup's transistors conducts current during its associated horizontal segment as well as all during its associated sloping segment.

(c) Exemplary claim 48 defines a:

"lamp assembly ... wherein the first transistor is characterized by having a pair of control terminals across which is applied a control voltage having a peak-to-peak magnitude substantially larger than twice the forward voltage drop of an ordinary semiconductor junction".

This feature is neither described nor suggested by either Dale or Canup.

If Examiner were to maintain his position to the contrary, he is requested to point out exactly where and/or how Dale and/or Canup suggests this particular feature.

In this connection, Applicant informs Examoner to the effect that -- by virtue of his drive transformer -- the drive voltage supplied to the bases of Canups' transistors must have a substantially symmetrical waveform; which, since the positive magnitude of the base-emitter voltage can not exceed one forward voltage drop of a semiconductor junction, means that the negative magnitude can not exceed one such forward voltqage drop either; which therefroe means that the peak-to-peak magnitude of Canup's drive voltage is equal to (i.e., not larger than) twice the forward voltage drop of a semiconductor junction.

RE AMENDMENTS

Claims 47-55 have all been amended; which amendments were made to more clearly distinguish the claimed invention from the teachings of the applied references.

RE NEW CLAIMS

New claims 56-64 have been constructed so as to patentably distinguish over the cited references.

Exemplary new claims 56-57 further exploits the feature otherwise defined by allowed claim 50.

Exemplary new claim 61 defines certain structural features of Applicant's invention not suggested by any of the cited prior art.

Exemplary new claim 62 defines Applicant's invention to have a transistor conducting once each period for a total duration distinctly shorter than half that of a complete cycle.

AMENDED CLAIMS in Serial No. 07/933,891

1 4. (Amendment) A lamp assembly operable to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals;

base means operable to be inserted into and held by the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means also including a combination of:

(a) rectifier means connected with the base electrodes and operative, whenever the base means is indeed inserted into the Edison-type lamp socket, to provide a DC voltage at a set of DC terminals;

(b) inverter means connected with the DC terminals and operative to provide an inverter voltage from a pair of inverter terminals; the inverter voltage having a fundamental period consisting of four time segments: (i) a first time segment during which the magnitude of the inverter voltage remains at a first substantially constant level, (ii) a second time segment during which the magnitude of the inverter voltage increases in a substantially gradual manner, (iii) a third time segment during which the magnitude of the inverter voltage remains at a third substantially constant level, and (iv) a fourth time segment during which the magnitude of the inverter voltage decreases in a substantially gradual manner; the inverter means including: (i) a first transistor characterized by conducting current during the first time segment but not during more than half of the second time segment, nor during any [at] other time[s], and (ii) a second transistor characterized by conducting current during the third time segment but not during more than half of the fourth time segment, nor during any [at] other time[s]; the duration of the first time segment being: (i) approximately equal to that of the third time segment, and (ii) distinctly shorter than half the duration of the fundamental period;

(c) current-limiting means connected between the inverter terminals and a pair of output terminals; and

(d) connect means operative to connect the output terminals with the lamp terminals.

2 4/8. The lamp assembly of claim 1 4/7 wherein the first transistor is characterized by having a pair of control terminals across which is applied a control voltage having a peak-to-peak magnitude substantially larger than twice the forward voltage drop of an ordinary semiconductor junction.

3 4/3. The lamp assembly of claim 1 4/1 wherein the inverter voltage has a peak-to-peak magnitude equal to the magnitude of the DC voltage.

4 5/0. The lamp assembly of claim 1 4/1 wherein the two transistors are series-connected across the DC terminals.

5 5/1. (Amended) A lamp assembly operable to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals; and

base means operable to be inserted into and held by the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means also including a combination of:

(a) rectifier means connected with the base electrodes and operative, whenever the base means is indeed inserted into the Edison-type lamp socket, to provide a DC voltage at a set of DC terminals;

(b) inverter means connected with the DC terminals and operative to provide an inverter voltage from a pair of inverter terminals; the inverter voltage having a fundamental period consisting of four time segments: (i) a first time segment during which the magnitude of the inverter voltage remains at a first substantially constant level, (ii) a second time segment during which the magnitude of the inverter voltage increases in a substantially gradual manner, (iii) a third time segment during which the magnitude of the inverter voltage remains at a third substantially constant level, and (iv) a fourth time segment during which the magnitude of the inverter voltage decreases in a substantially gradual manner; the inverter means including a first transistor characterized by conducting current in its forward direction during [at least part of] the first time segment; the duration of the first time segment being: (i) approximately equal to that of the third time segment, and (ii) [significantly] <u>distinctly</u> shorter than half the duration of the fundamental period; the first transistor being operative to prevent the flow of current in its forward direction during <u>at least a significant part of each of</u> the second and fourth time segments;

(c) current-limiting means connected between the inverter terminals and a pair of output terminals; and

(d) connect means operative to connect the output terminals with the lamp terminals.

6 52. (Amended) A lamp assembly adapted to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an ordinary AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having two lamp terminals; and

base means operable to be inserted into the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means including frequency-converting ballast means connected in circuit between the base electrodes and the lamp terminals; the ballast means being operative to provide an AC voltage to the lamp terminals; the ballast means being characterized by including a periodically conducting first transistor having: (i) a pair of control input terminals receiving a control signal, and (ii) a pair of output terminals across which exists a periodically varying transistor voltage; the periodically varying transistor voltage being characterized by having a fundamental period consisting of four time segments: (i) a first time segment during which the magnitude of the transistor voltage remains at a first substantially constant level, (ii) a second time segment during which the magnitude of the transistor voltage increases in a substantially gradual manner, (iii) a third time segment during which the magnitude of the transistor voltage remains at a third substantially constant level, and (iv) a fourth time segment during which the magnitude of the transistor voltage decreases in a substantially gradual manner; the transistor conducting current in its forward direction during at least part of the first time segment but not during most of the second time segment.

cont.

7 53. (Amended) The lamp assembly of claim 6 52 wherein the control signal has a peak-to-peak magnitude [substantially] distinctly larger than twice the forward voltage drop of an ordinary semiconductor diode junction.

8 54. (Amended) The lamp assembly of claim 6 52 wherein the duration of the first time segment is [significantly] distinctly shorter than half the duration of the fundamental period.

9 55. (Amended) The lamp assembly of claim 6 52 wherein no current flows through the first transistor during any part of the fourth period.

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56. The lamp assembly of claim 52 further characterized by including: (i) a pair of terminals across which exists a DC voltage; and (ii) a second transistor series-connected with the first transistor to form a series-combination, which series-combination being connected across the DC terminals.

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57. A lamp assembly adapted to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an ordinary AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals; and

base means operable to be inserted into and held by the Edison-type lamp socket; the base means including base electrodes operable to make electrical contact with the socket electrodes; the base means also including a sub-assembly connected in circuit between the base electrodes and the lamp terminals; the sub-assembly being functional, as long as the base electrodes do indeed make electrical contact with the socket electrodes, to provide a lamp AC voltage to the lamp terminals; the frequency of the lamp AC voltage being distinctly higher than that of the AC power line voltage; the sub-assembly being further characterized by including: (i) a pair of DC terminals across which exists a DC voltage; and (ii) two periodically conducting transistors series-connected across the DC terminals.

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58. The lamp assembly of claim 57 wherein the base means is further characterized in that the absolute magnitude of the DC voltage is distincly higher than the peak absolute magnitude of the AC power line voltage.

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59. The lamp assembly of claim 57 wherein the gas discharge lamp includes plural parallel-disposed cylindrically-shaped lamp-segments protruding out from the base means and is further characterized by not having any non-translucent object mounted in between the cylindrically-shaped sections.

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60. The lamp assembly of claim 57 wherein: (i) the base means includes a cylindrically-shaped screw-type plug; and (ii) the gas discharge lamp includes at least one cylindrically-shaped lamp-segment having its cylindrical axis disposed parallel to the cylindrical axis of the cylindrically-shaped screw-type plug.

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15 61. The lamp assembly of claim 11 wherein the base means includes a housing structure onto one side of which is mounted the gas discharge lamp and onto the opposite side of which is mounted a cylindrically-shaped screw-type plug screwed into the lamp socket; the screw-type plug having (i) a cylindrical axis, and (ii) a maximum screw-base diameter; the cylindrical axis constituting an axis of symmetry for the base means; which base means further characterized by having a maximum diameter no larger than about 2.5 times the maximum screw-base diameter.

16 62. A lamp assembly operable to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals; and

base means operable to be inserted into and held by the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means also including a combination of:

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(a) rectifier means connected with the base electrodes and operative, whenever the base means is indeed inserted into the Edison-type lamp socket, to provide a DC voltage between a pair of DC terminals;

(b) inverter means connected with the DC terminals and operative to provide an AC inverter voltage from a pair of inverter terminals; the AC inverter voltage having a fundamental cycle period; the AC inverter voltage being further characterized by being of frequency distinctly higher than that of the AC power line voltage; the inverter means including a first transistor characterized by conducting current in its forward direction for but a brief period once during each fundamental cycle period; the duration of the brief period being distinctly shorter than half the duration of the fundamental cycle period.

17 63. The lamp assembly of claim 16 further characterized in that the inverter means includes a second transistor series-connected with the first transistor to form a series-combination, which series-combination is connected across the DC terminals.

18 64. The lamp assembly of claim 16 further characterized in that the absolute magnitude of the DC voltage is distinctly higher than the peak absolute magnitude of the AC power line voltage.